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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,986	09/12/2003	Louis K. Scheffer	CA7016672001	6083

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,986	SCHEFFER, LOUIS K.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6,7,12,13,17,18,23,24,28,29 and 34-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,7,12,13,17,18,23,24,28,29 and 34-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/660,986 and amendment filed on 7/19/2005. Claims 1-2, 6-7, 12-13, 17-18, 23-24, 28-29 and 34-57 remain pending in the application.

Claim Objections

2. Claims 6, 17, 28, 40-41, 47, 49 and 56-57 are objected to because of the following informalities: these claims have claimed dependency problems because they should not depend on canceled claims. Phrases "**a predicted effect**" and "**one or more parameters** of the design" in claims 6, 17 and 28, where a predicted effect and one or more parameters needed to clearly specified; and "examining **effects** of the clock element modification and placement locations as a **mixed programming problem**" in claims 40-41, 47, 49, and 56-57, where effects and mixed programming problem needed to clearly defined. Appropriate correction is required in order to avoid claimed construction problem.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 12 and 23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation of "automatically modifying a number of clocked elements in the one or more pipeline locations of the design" is clearly described in the specification.

Claims 1, 12 and 23 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The steps how to perform automation are critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). Without the essential steps showing how the automation of modification can be performed, the claimed invention is not enabling one to make and use the claimed invention.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 12-13, 23-24, 34-38, 42-45, and 50-54 are rejected under 35 U.S.C. 103(a) as being obvious over Smits et al. (6,631,444).

6. As to claims 1, 12 and 23, Smits et al. teach an IC design that provides a solution to a synchronization and timing problems inherent in the IC design of a very large, on-die memory operating with a high-speed processor core in pipelined fashion (see field of the invention, col. 2, lines 39-58, and Fig. 2, 4-5 and its detailed description). The problems arise when some of the banks are located relatively close to central location and other banks are located relatively far from central location (col. 5, lines 60-67, col. 3, lines 20-33). In order to resolve synchronization and timing problems along bus lines operating in pipelined fashion, Smits et al. teach inserting number of flip-flips, buffers or latches along the bus lines (rules for pipelining) or at specified one or more pipeline locations of the IC design (electronic design) (Fig. 4-5, col. 5 line 60 to col. 7 line 30). Thus, Smits et al. teach generating an electronic design (IC design); specifying one or more pipeline locations and modifying a number of clocked elements in the one or more pipeline locations. Because latency to/from all cache banks is made to be identical in the architecture of the present invention, data accesses can be pipelined,i.e., continuous read and write operations can be performed regardless of which bank the data is actually located. Output data flows back the processor core in the same order it was requested irrespective of the location of the cache bank on the chip where the data is physically stored (col. 7 lines 1-29). Smits et al. do not explicitly automatically inserting (modifying) number of clocked elements in interconnect pipelining. Automation method is known to be more convenient routine practice and fast. Therefore, it would have been obvious to practitioners that the insertion of number of clocked elements in the interconnect pipelining (modifying number of inserted clocked elements) as taught

by Smits et al. would have been done automatically because it is more convenient and fast, thereby it would equally provide synchronization and latency.

7. As to claims 2, 13 and 24, Smits et al. teach organizing signals in the electronic design into groups (input data/address paths) (col. 6 lines 30-34; Fig. 4-5) and specifying rules for pipelining (col. 6, lines 1-9, number of inserted flip-flops, buffers or latches).

8. As to claims 34-38, 42-45 and 50-54, Smits et al. the architecture for a cache memory fabricated on a die with a processor (CPU) including inserted number of clocked elements in interconnect pipelining in according with various physical distances that each of the banks located on the die relative to the central location associated with data transmission from/to the processor core within a given clock cycle, and also operating frequency (Figs. 4-5, the insertion of number clocked elements or flip-flops can done manually or automatically; col. 5 line 30 to col. 7 line 30).

9. Claims 6-7, 17-18, 28-29, 39-41, 46-49 and 55-57 are rejected under 35 U.S.C. 103(a) as being obvious over Smits et al. (6,631,444) in view of Yoshikawa (6,466,066).

10. As to claims 6-7, 17-18 and 28-29, Smits et al. teach inserting number of clocked elements in the one or more pipeline locations of IC design in order to provide synchronization and in compliance with timing constraints using placement tool (using well known automated layout tool in IC design layout), where the number of inserted clocked elements are based on distances (parameter, length parameters, placement position) between banks and processor core and operating frequency (Fig. 4, col. 5 line 30 to col. 7 line 30), to thereby insure that all data arrives and is latched at the central

location at a predetermined time regardless of which bank the data is actually stored in (col. 6 lines 51-58). It well known to one ordinary skill in the art that when inserting clocked elements in interconnect pipelining as taught by Smits et al. there some effects from such modifications. In addition, Yoshikawa teach insertion of clocked elements in interconnect pipelining (modification or adjustment), there are some effect (influence) from such modification, so that adjustment of the inserted clocked element can be made in order to minimize the effect or influence of the modification (col. 3 line 1 to col. 16 lines 46). With that motivation and expected results, it would have been obvious to one of ordinary skill in the art at the time the invention was made to take consideration of the effect that the clocked element modification has one or more parameters of the design to thereby minimize the effect from skew (col. 4 lines 45-56, abstract).

11. As to claims 39, 46 and 55, Smits et al. operating frequency and an efficiency per cycle (col. 7 lines 10-30; col. 6 lines 23-58).

12. As to claims 40, 47 and 56, Smits et al. teach insertion number of clocked elements in the one or more pipeline locations of IC design in order to provide synchronization and in compliance with timing constraints using placement tool (well known automated layout tool in IC design layout), where the number of inserted clocked elements are in function of physical distances (parameter, length parameters) between banks and processor core, and also operating frequency (Fig. 4, col. 5 line 30 to col. 7 line 30), to thereby insure that all data arrives and is latched at the central location at a predetermined time regardless of which bank the data is actually stored in (col. 6 lines 51-58). In order to obtain such insurance that all data arrives and is latched at the

central location at a predetermined time regardless of which bank the data is actually stored in, it would have been obvious to practitioners in the art at the time the invention was made to examine the effects on the one or more parameters, wherein the clocked element modification and parameter effect examination is iteratively performed because the examination would make any necessary adjustment of the insertion of the clocked elements thereby synchronization and latency would be warranted.

13. As to claims 41, 48-49 and 57, Smits et al. teach inserting number of clocked elements in the one or more pipeline locations of IC design in order to provide synchronization and in compliance with timing constraints using placement tool (well known automated layout tool in IC design layout), where the number of inserted clocked elements are in function of physical distances (parameter, length parameters) between banks and processor core, and also operating frequency (Fig. 4, col. 5 line 30 to col. 7 line 30), to thereby insure that all data arrives and is latched at the central location at a predetermined time regardless of which bank the data is actually stored in (col. 6 lines 51-58). In order to obtain such insurance that all data arrives and is latched at the central location at a predetermined time regardless of which bank the data is actually stored in, it would have been obvious to practitioners in the art at the time the invention was made to examine effects of the clock element modification and placement location as a mixed programming problem because the examination would make any necessary adjustment of the insertion of the clocked elements including selecting appropriate clocked elements to thereby providing synchronization and latency.

Remarks

14. Applicant argued that Smits et al. inserting clocked elements manually, not automatically. Regarding to this manner, Examiner respectively submits that automated insertion of clocked elements in an interconnect pipelining as taught by Smits could have been done manually or automatically. The claim recited "automatically modifying..." would have obvious to one having ordinary skill in the art at the time the invention was made, since it has been held that an automatic means to replace manual activity which has accomplished the same result involves only routine skill in the art. *In re Venner*, 120 USPQ 192.

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER